WHAT IS CLAIMED IS

1. A semiconductor memory device, comprising:

a data buffer for inputting/outputting data from/to an exterior of the device;

a plurality of DRAM cell array blocks;

an SRAM redundancy cell disposed peripheral portion of said plurality of DRAM cell array blocks;

a fuse circuit which stores an address of a defect memory cell in the DRAM cell array blocks;

a comparison circuit which compares an input address with the address stored in said fuse circuit; and

an I/O bus which couple said SRAM redundancy cell to said data buffer in response to an address match signal from said comparison circuit.

2. The semiconductor memory device as claimed in claim 1, further includes a sense amplifier line that is provided for each of said plurality of DRAM cell array blocks, wherein said SRAM redundancy cell is provided in part of an area generally allocated said sense amplifier line.

3. The semiconductor memory device as claimed in claim 1, further includes a sub-word

decoder that is provided for each of said plurality of DRAM cell array blocks, wherein said SRAM redundancy cell is provided in part of an area generally allocated to said sub-word decoder.

4. The semiconductor memory device as claimed in claim 1, further comprising a sense amplifier line and a sub-word decoder that are provided for each of said plurality of DRAM cell array blocks, wherein said SRAM redundancy cell is provided at a cross section where an extension of said sense amplifier line and an extension of said sub-word decoder intersect.

5. The semiconductor memory device as claimed in claim 1, further comprising a word strap area that is provided for each of said plurality of DRAM cell array blocks, wherein said SRAM redundancy cell is situated in part of an area generally allocated to said word strap area.

6. The semiconductor memory device as claimed in claim 1, further comprising a sense amplifier line and a word strap area that are provided for each of said plurality of DRAM cell array blocks, wherein said SRAM redundancy cell is situated at a cross section where an extension of said sense amplifier line and an extension of said

word strap area intersect.

7. The semiconductor memory device as claimed in claim 1, further comprising a column decoder that is provided for each of said plurality of DRAM cell array blocks, wherein said SRAM redundancy cell is situated in part of an area generally allocated to said column decoder.

8. The semiconductor memory device as claimed in claim 1, further comprising a word decoder that is provided for each of said plurality of DRAM cell array blocks, wherein said SRAM redundancy cell is situated in part of an area generally allocated to said word decoder.

9. The semiconductor memory device as claimed in claim 1, wherein said SRAM redundancy cell which is situated around each of said plurality of DRAM cell array blocks has a memory capacity for replacing a single defect location in the DRAM cell array blocks.

10. The semiconductor memory device as claimed in claim 9, wherein said SRAM redundancy

cell is capable of replacing a defect memory cell located in any one of said plurality of DRAM cell array blocks.

11. The semiconductor memory device as claimed in claim 10, wherein said fuse circuit is set such that when two or more defect locations are present in one of the DRAM cell array blocks, at least one of the defect locations is replaced by said SRAM redundancy cell of another one of the DRAM cell array blocks.

12. The semiconductor memory device as claimed in claim 1, wherein said comparison circuit compares a row address, a block address, and a column address of said input address with the address stored in said fuse circuit.

13. The semiconductor memory device as claimed in claim 12, further comprising:

a word decoder which selectively activates a word line corresponding to the row address of said input address regardless of the comparison made by said comparison circuit;

a column decoder which selectively activates a column line corresponding to the column address of said input address in response to an unmatched result found by said comparison circuit,

and selectively activates a redundant column line corresponding to said SRAM redundancy cell in response to the address match found by said comparison circuit.

14. The semiconductor memory device as claimed in claim 13, wherein a number of bits of SRAM redundancy cells selected by said redundant column line is equal to a number of bits of data selected by said column line.

15. The semiconductor memory device as claimed in claim 1, further comprising:

a sense amplifier line that is provided for each of said plurality of DRAM cell array blocks; and

a word decoder that is provided for each of said plurality of DRAM cell array blocks,

wherein said SRAM redundancy cell is situated at a cross section where an extension of said sense amplifier line and an extension of said word decoder intersect.